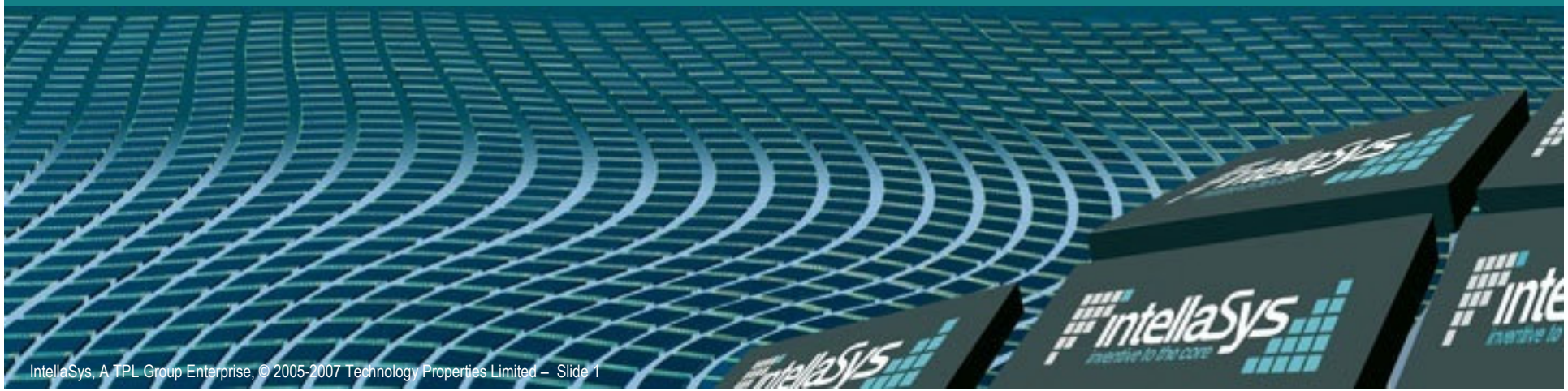
IntellaSys
inventive to the core

Imagine a SEA™ of Processors



Remember when…

- TPL began development and marketing of proprietary product technology in 1988 – first licensee was Harris Corp in 1989
- IntellaSys was formed by TPL in 2003 to develop, build and sell high-speed multi-core processor arrays
- Alliacense was formed by TPL in 2004 to sell & manage proprietary product technology – Intel purchased the first license in 2005
- SEAforth-24 wins Portable Design Editor's Choice award for 2006

IntellaSys

- ~100,000 sq ft
- 200+ employees
- 8 Design Centers
  - Cupertino, CA
  - Irvine, CA
  - Tempe, AZ
  - Castle Rock, CO
  - Redding, CA
  - Cincinnati, OH
  - Vienna, Austria
  - Chennai, India
- International Sales Offices
  - Lugano, Switzerland
  - Taipei, Taiwan

The Towers – Cupertino City Center

You've probably been reading about us

2006 Press Coverage of SEAforth

Remember when…

- Embedded processors were just I/O "bit bangers?"
- When "high-speed serial link" meant 9600 baud?
- When the most complex algorithm chips had to run was calculating a CRC?
- Airliners had propellers?

Today's processors…

- Still do all the I/O bit-banging of the old days, BUT NOW THEY HAVE TO DO…
- High-speed serial data links at GIGABIT rates
- Multiple algorithms at the SAME time
- Algorithms like H.264 and MPEG-II for HighDef TV

… and they do it in environments where…

- Standards are changing faster than the chips
- Consumer demands dictate LOW cost with a bare minimum number of chips
- Applications are mobile and require low power

Problem with current embedded processors is the Processor Speed

- 400MHz CPU is far too slow
- Slow processor forced to pass all data and code over a single bus prevents the CPU from doing the I/O in a simple, programmed manner
- If you could speed the processor (and bus) up sufficiently the need for specialized I/O would largely go away

What is the REAL I/O Problem?

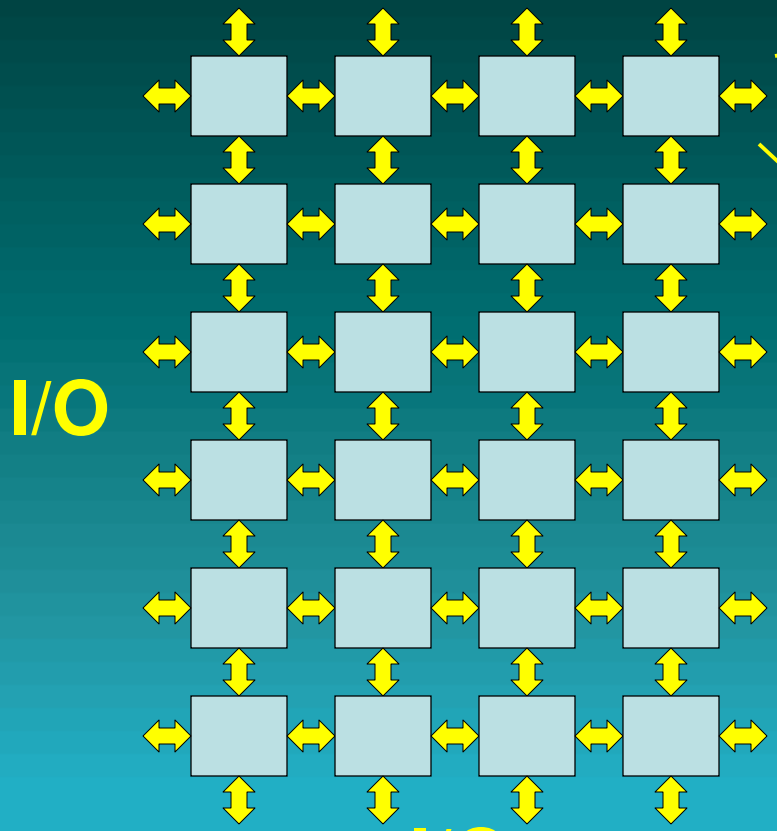
Typical Input requiring DSP

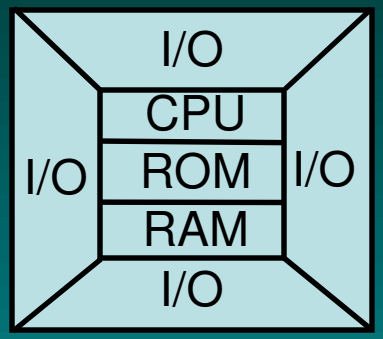
To the bus via DMA

All external signals go through analog PHYs even if they're already digital

If the processor were fast enough to do the UART function AND act as a DSP AND do all of the other processing for all the other signals, there would be no need for a custom chip

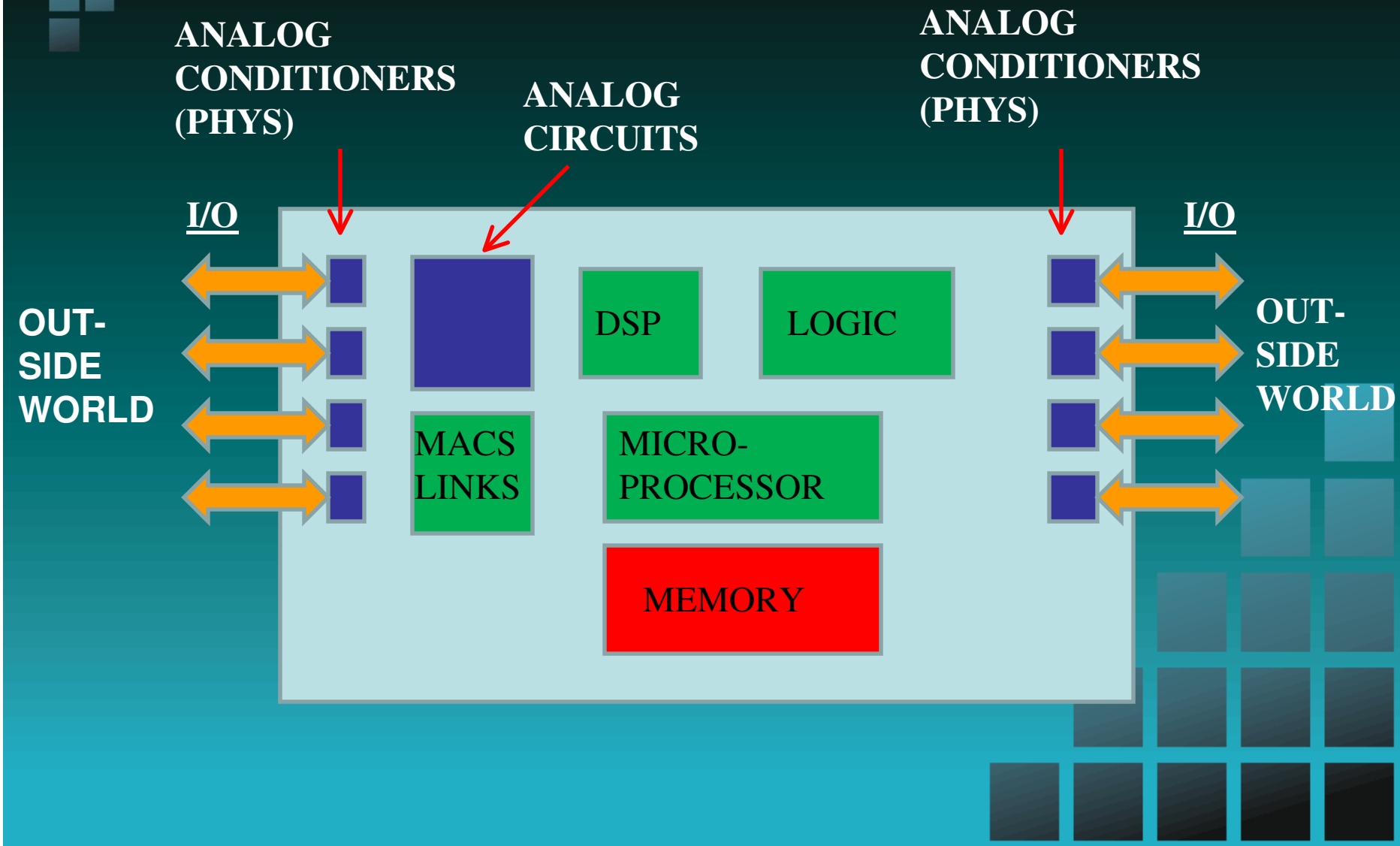
There are no processors that fast, but… what if you put a whole bunch of them on one chip??



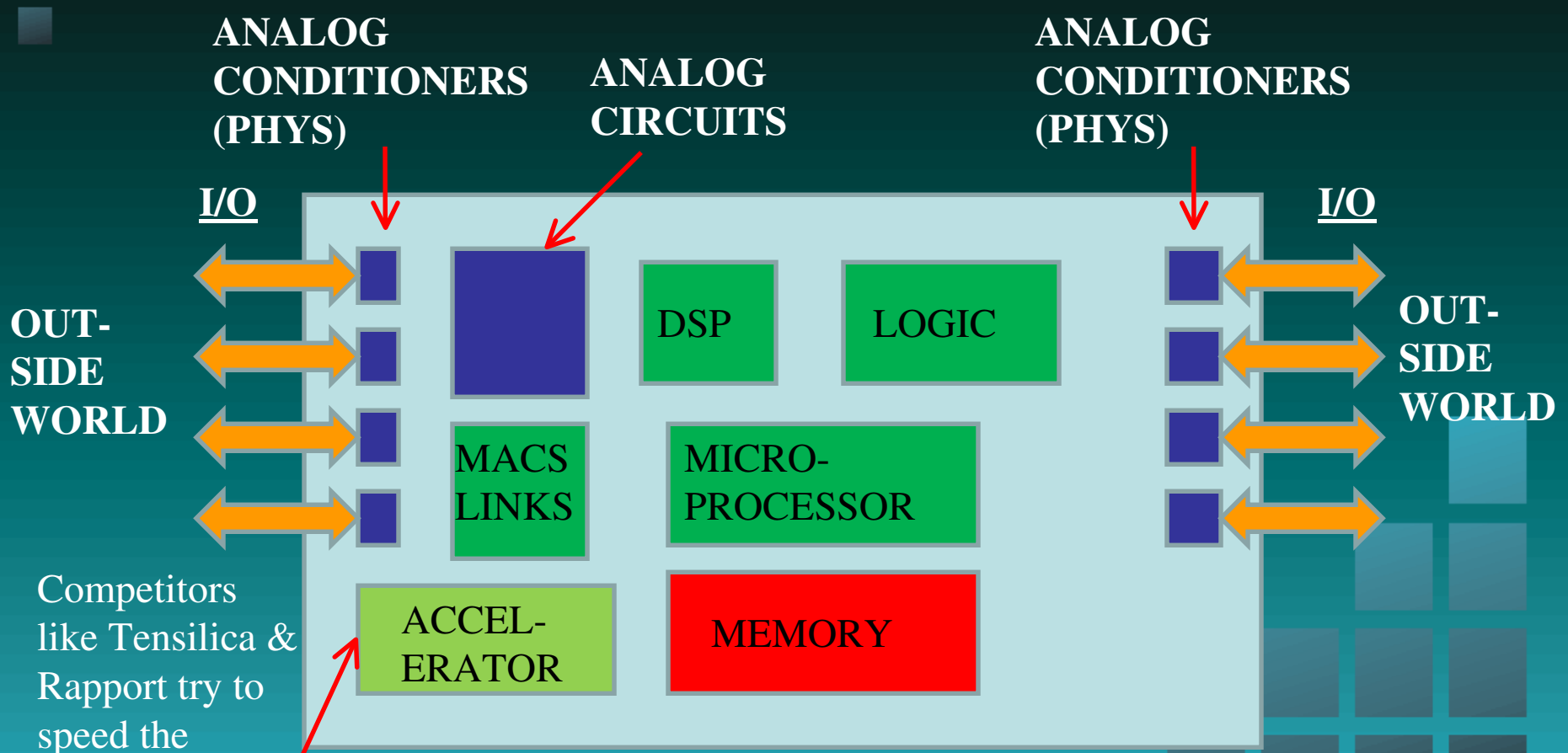


- All cores identical
- Each is complete with CPU, ROM, RAM and I/O
- Cores in the middle use I/O to talk to each other

System From the Top



Competitors Try to Speed Up the System

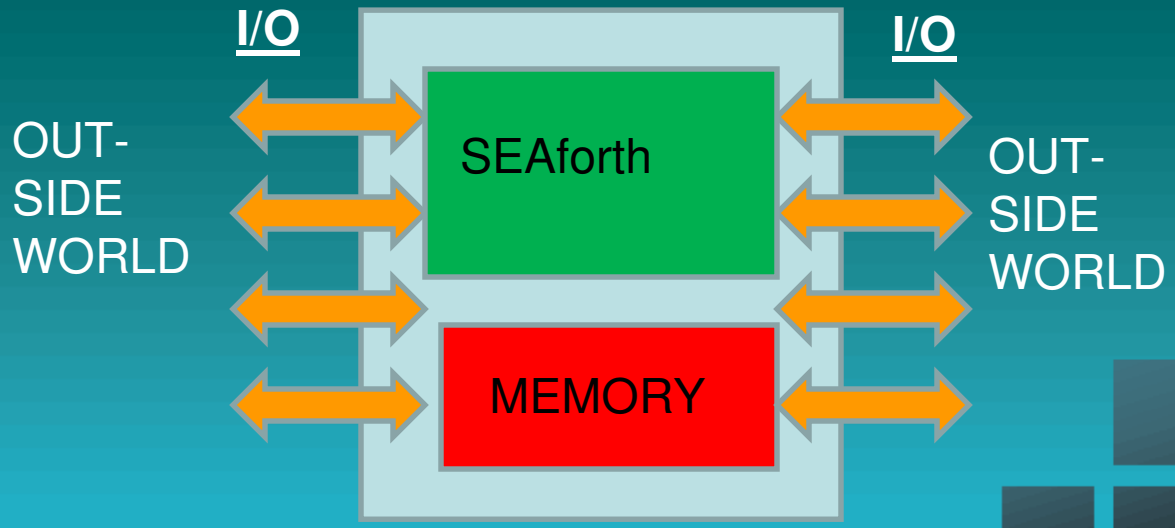


Competitors like Tensilica & Rapport try to speed the system up by adding chips

In most cases this has limited effect and only adds to the cost and complexity of the system

SEAforth Goals

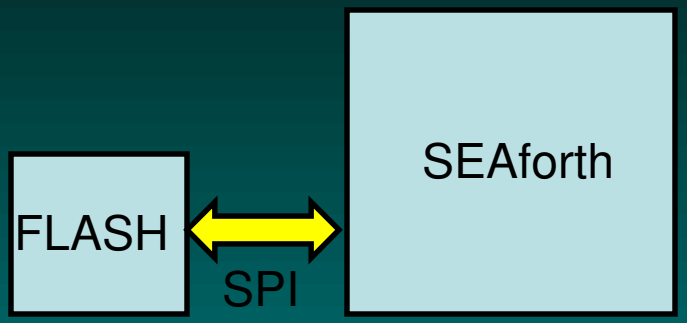
- Replace all chips except RAM
- Increase Performance
- Dramatic cost reduction
- Universal off-the-shelf parts



SEAforth Super Performance

- Each core runs at 1GHz… one Billion VentureForth instructions per second
- 24 cores = 24 Billion instructions per second
- No bus bottleneck because there is no bus
- No shared memory bottleneck because there is no shared memory
- Cores cooperate on tasks… use several as a DSP function, a handful for MP3 or H.264
- I/O pins are programmable for max flexibility

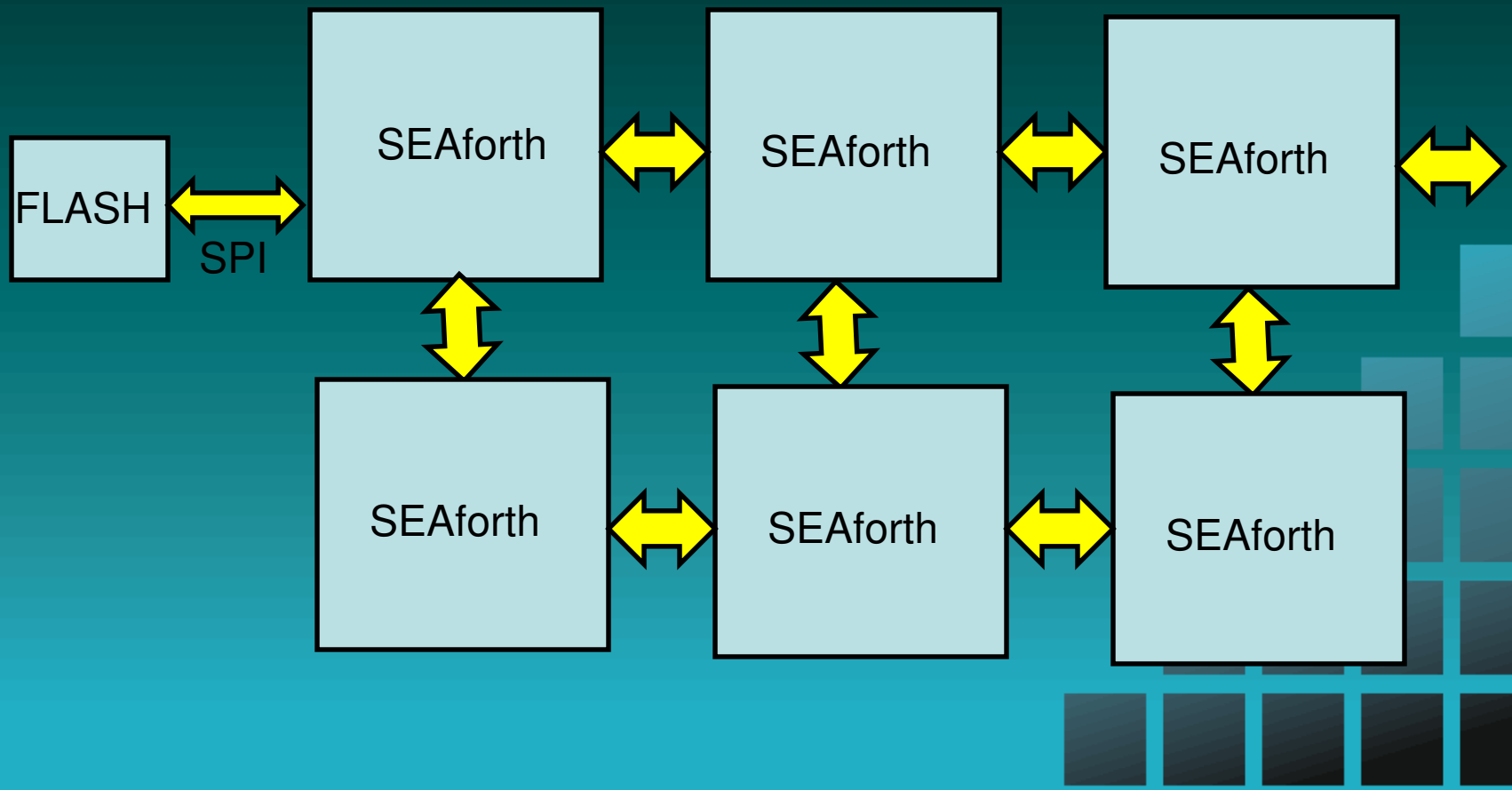
Programs in RAM



- Customer applications code and data run from each core's RAM
- SEAforth loads code from FLASH during boot
- Ripple loads all of the cores with their appropriate code

- Feature changes occur in software in FLASH memory chips
- Application changes made WITHOUT mask changes / $$$ charges
- Same SEAforth chip can function as the System on a Chip (SOC) for customer's entire product line

Expanding the SEAforth Array



What is a core processor?

- 18-bit dual stack oriented engine – a Turing machine
- Runs VentureForth, a 32 instruction RISC language
- Each word contains four instructions
- Instruction execution time approx 1ns
- 64 - 128 words of ROM containing BIOS. Each core processor has its own version of the BIOS
- 64 - 128 words of RAM containing program and data
- Clock (each core processor has its own 1GHz ring oscillator)
- Four communications (and I/O) registers

Cores execute code from 3 places

- ROM BIOS
  - Default I/O configuration & drivers
  - Math and other “helper” routines
  - Routing routines for message and data
  - Each core has BIOS unique to it
- RAM
  - Applications code & data
- Ports
  - Boot from I/O port and pass data from core to core by executing transport code and then sending data
  - Run subroutines resident on a neighbor
  - Share data between neighbors

What can you do with 64 - 128 Words ?

- Each data word is 18 bits
- Each instruction word has FOUR instructions
  - 64 words = 256 instructions
  - 128 words = 512 instructions
- Executing from ports means sharing code
- Complex algorithms spread data over multiple cores
  - Matrix stores each row in separate core
- Incredible Code Packing Density
  - Random Number Generator … ONE instruction
  - FIR Filter – 22 instruction words
  - iDCT (Inverse Discrete Transform – 16 words

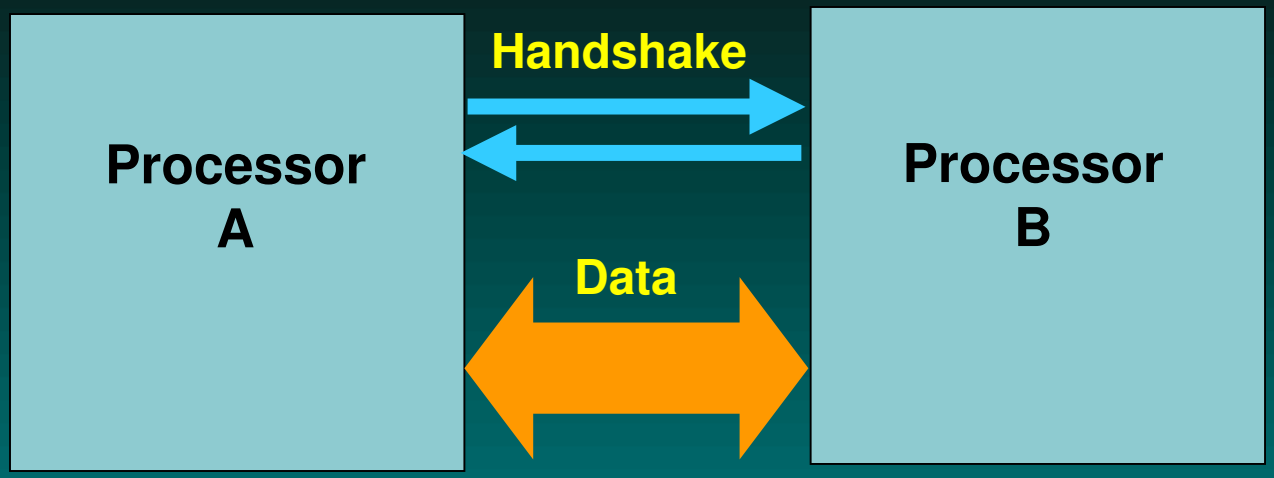
Processor cores used for…

- Algorithms and subroutines – dedicated processors mean no context switching time
- DSP functions like FFT and DFT
- “Interrupts” – assign a processor to each
- I/O ports driven by their processor which programs them to be SPI, SD, I^2C, a Real Time Clock or anything else you can think of
- Manage communication routes for communicating with other processors – be a “smart wire”

High-speed node to node communications

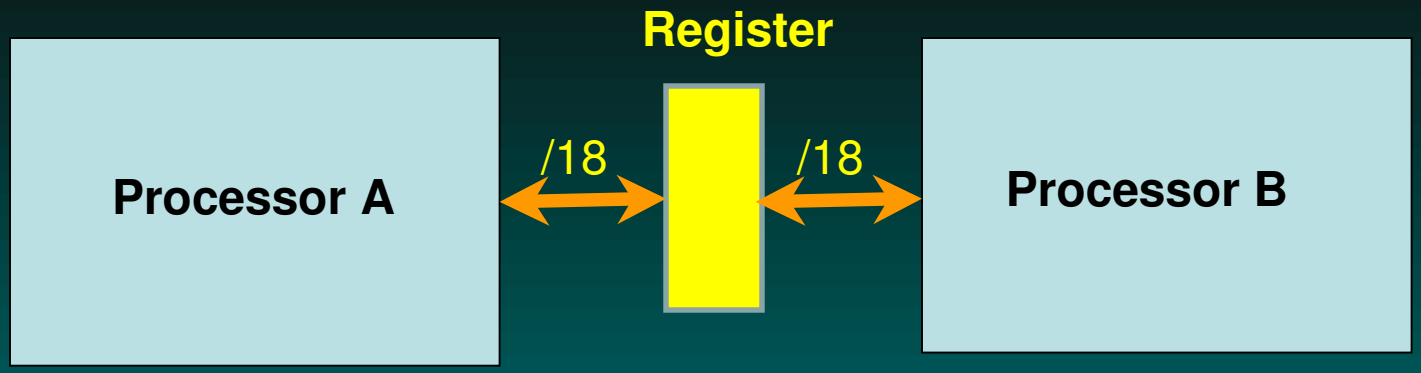
- Cores are constantly passing data back and forth, even sharing code
- Key to SEAforth efficiency is our straightforward way to do that
  - Nearest neighbors only
  - Extremely fast … 2ns per word transferred
- Multi-core algorithms require fast data transfers for video processing

Traditional way of transferring data



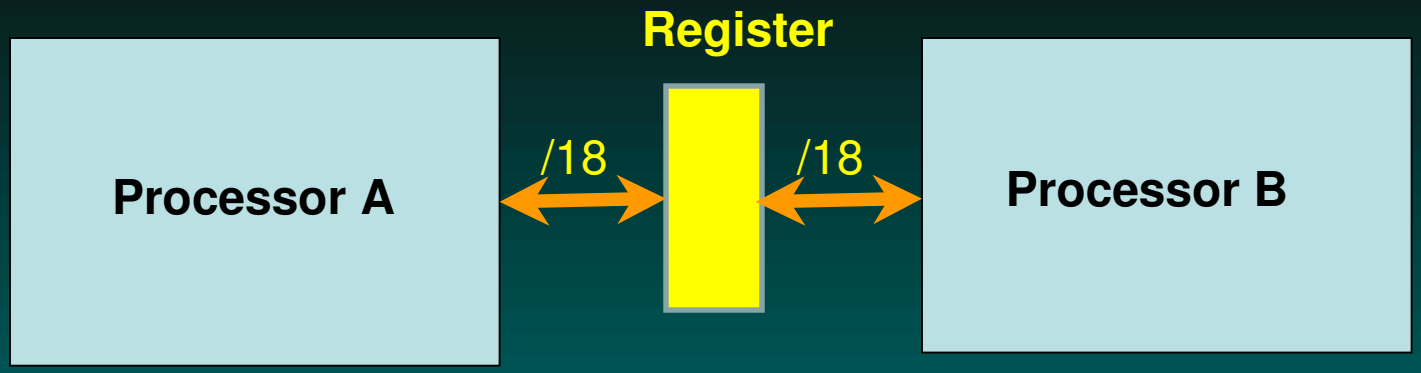
- Loop on handshake lines until Processor B ready to receive data
- Send data
- Loop on handshake lines until Processor A ready to send next word
- More time spent in handshake loops than in data transfer

SEAforth data transfers



- Processor A assumes B is always ready for data… does Send data, Send data, Send data
- Processor B assumes A is always sending fresh data… does Get data, Get data, Get data
- 18-bit transfers every 2ns (if processors are actually ready)
- No performance penalty in sharing code and memory
- Ideal for dataflow type applications

SEAforth - low power by design

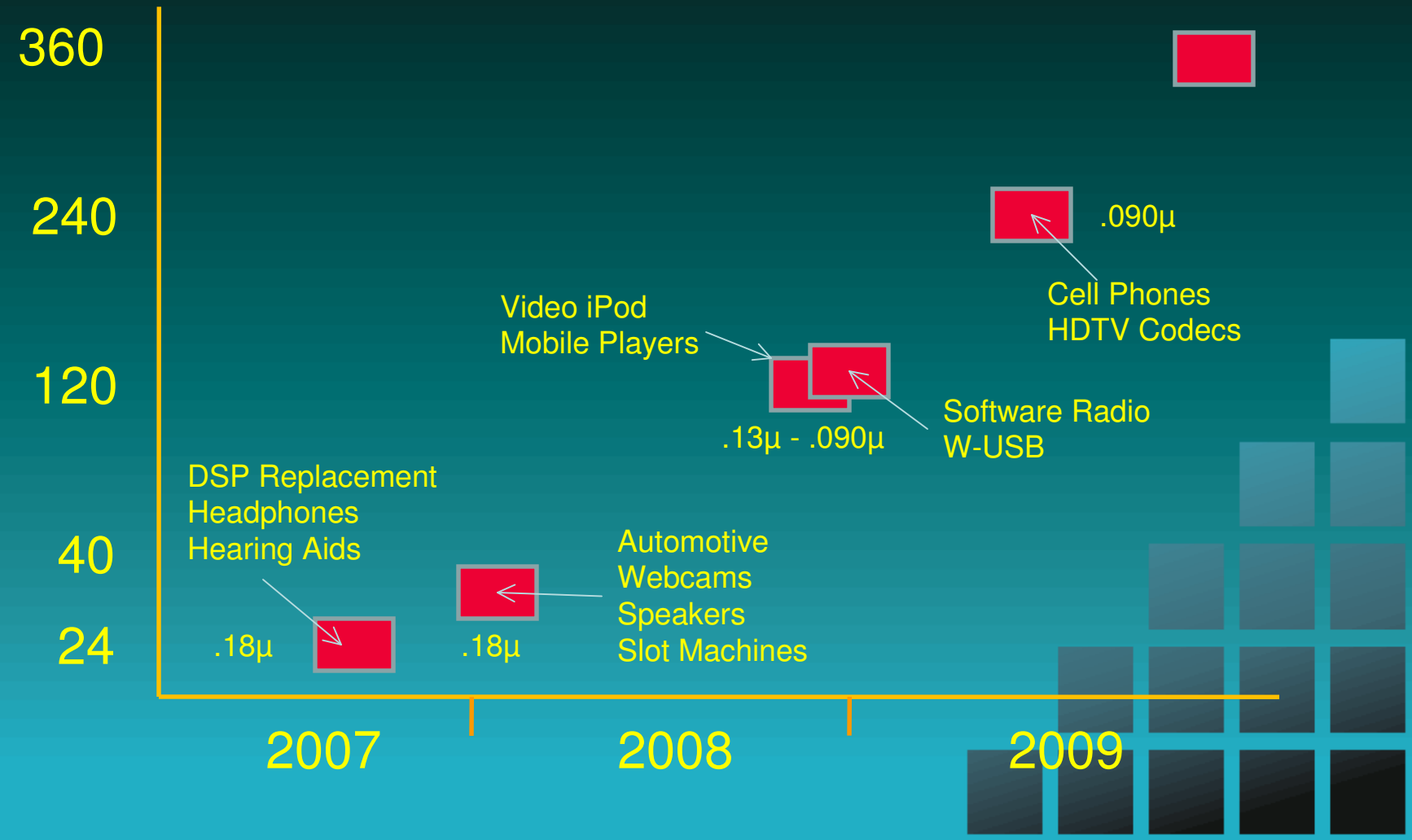


- Processor B sleeps, ZERO power, until A has fresh data to transfer
- Processor A sleeps, ZERO power, until B is ready for more data
- Typically 2/3 of nodes are sleeping at any instant and dissipating ZERO power
- At next instant, still 2/3 of nodes are sleeping, but it will be completely different set of nodes
- 9mW per core while running, .04mW while sleeping

SEAforth Family

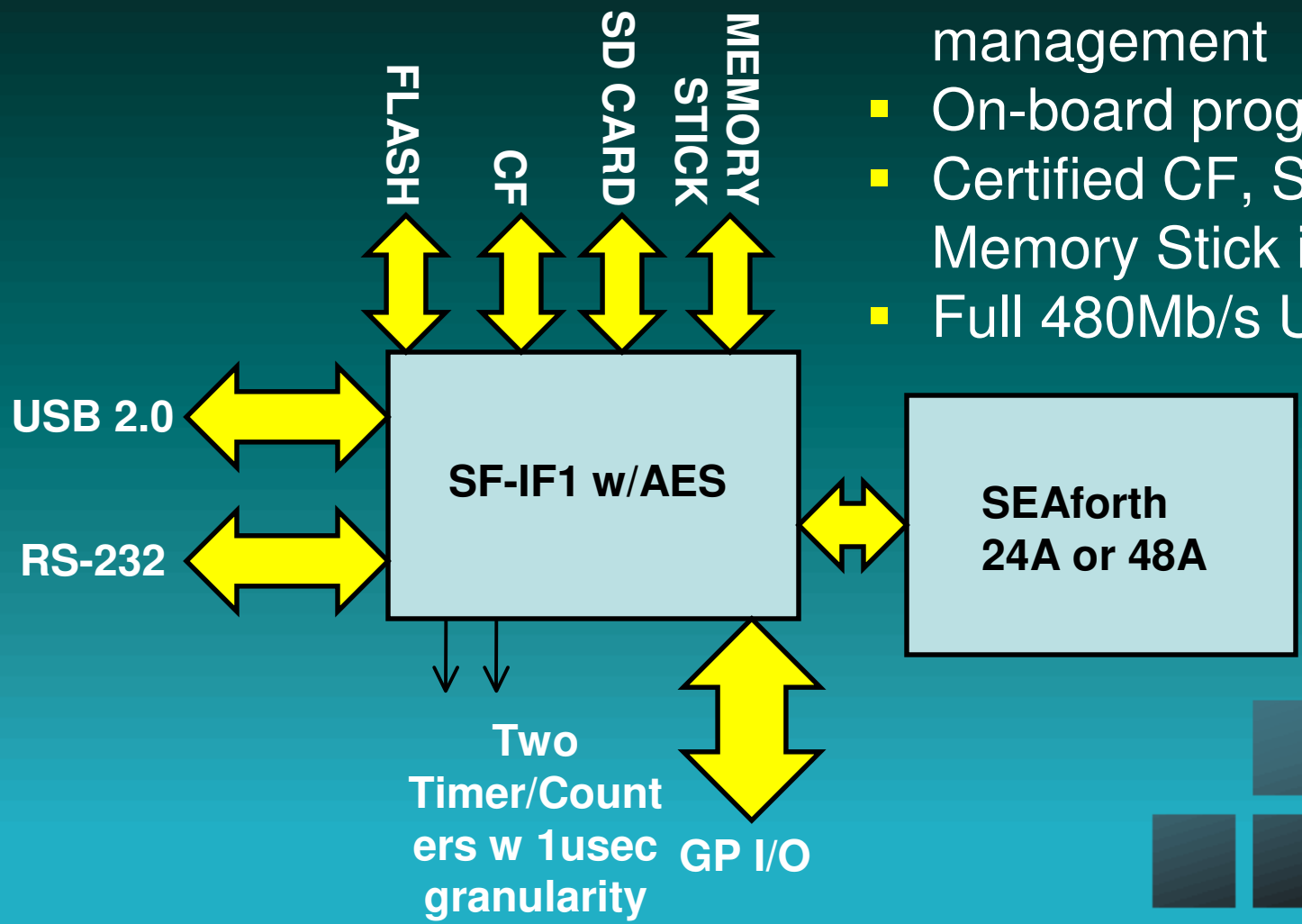
- SF-24A … 24 cores w/64 words each of RAM and ROM, low cost part. Sampling via thumb drives in Q3 - 2007
- SF-48A … 48 cores w/128 words each of RAM and ROM and extensive I/O. Sampling via “thumb” drives in Q1 - 2008
- SF-IF1 Universal Interface Chip... USB, RS-232, SD, Memory Stick, and Flash drivers plus AES engine and two clock timers. Certified by USB and Sony (Memory Stick), etc. Available August. Provides customers with way to program and manage Flash on their production boards.

SEAforth Roadmap



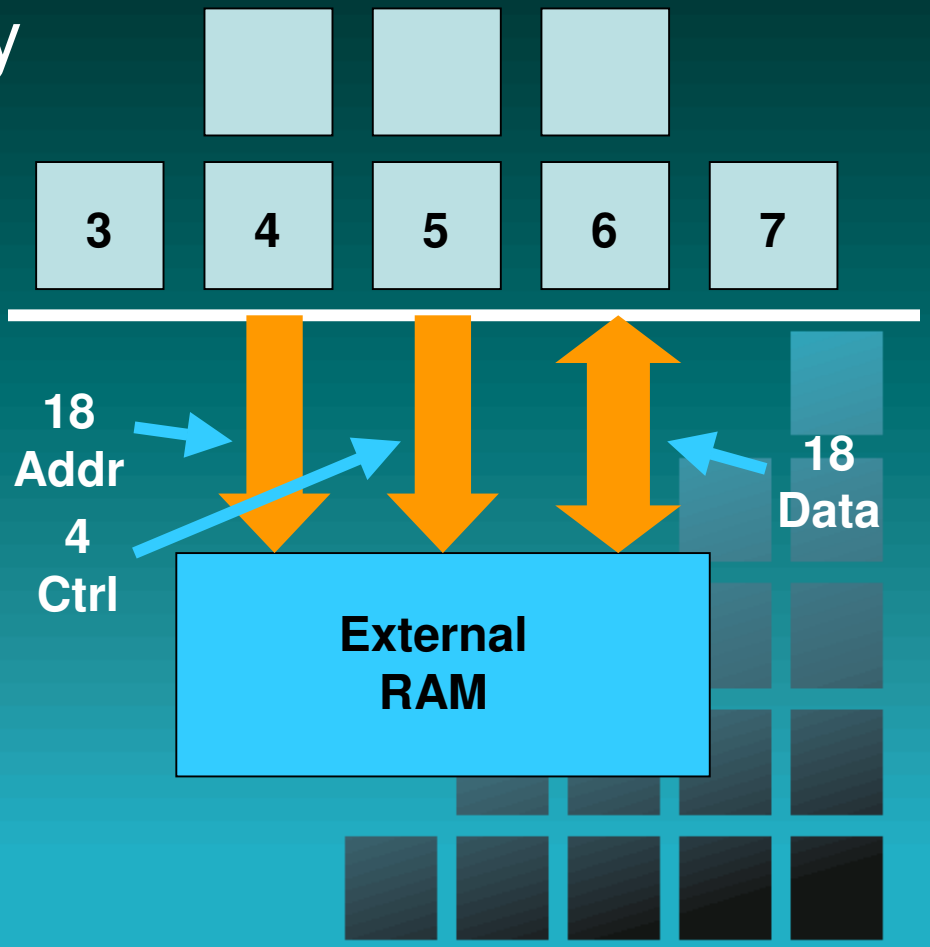
Using the SF-Universal Interface

- Provides FLASH management
- On-board programming
- Certified CF, SD, and Memory Stick interfaces
- Full 480Mb/s USB 2.0



SEAforth external memory

- 3 cores dedicated to handle external memory (static or dynamic)
- 1 Mword or 16 Mwords with paging
- 6 ns access
- Supplements internal RAM in each core
- Used for buffers
- Can also be used for large GP I/O interface



Analog functionality

- Two combination A/D and D/A converters
- Each can dynamically switch between A/D and D/A modes
- Can be used to xmit / receive wireless signals up to 20MHz
- 9-bit D/A drive inexpensive speakers and earphones directly
- 18-bit A/D for audio applicationsTw

Programming SEAforth

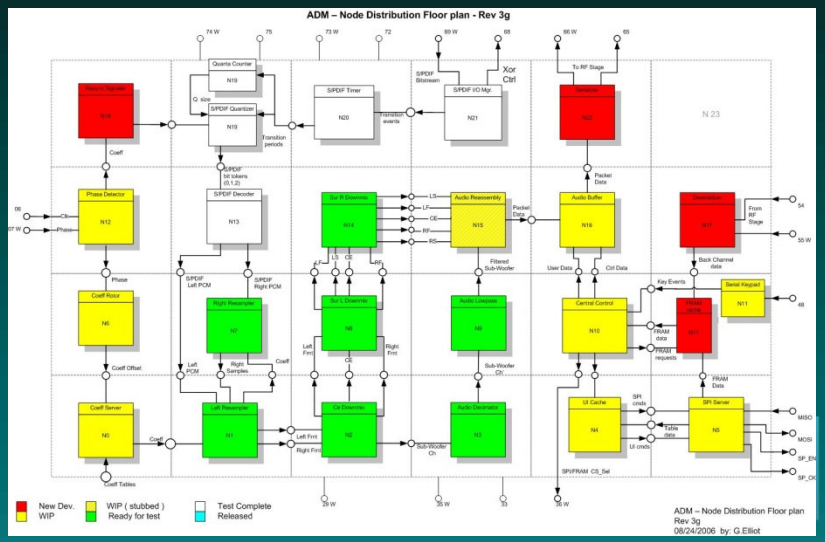
- VentureForth – RISC version of Forth
- 32 Instructions
- Four instructions per word
- microNEXT takes advantage of a four instruction "cache" by jumping back to the first instruction in a word implementing a fetch-less loop with spectacular performance in data pumps and when executing code directly from neighbors
- Portable Code
  - Can be moved from core to core, or from group of cores to group of cores
  - Can be moved from one chip to another
  - Replace two 24-core parts with one 48-core part

Software Modules for the SEAforth Library

- MP3 decode
- LCD screen drivers
- RF bidirectional links
- TCP/IP stack
- JPEG/GIF/PNG display
- H.264 codec (decode)
- ANS Forth interpreter
- Scriptable GUI generator

Building Applications

- Hook software modules together with glue code
- Library software modules
  - H.264, MP3, etc
- Build your own modules for your unique requirements
- With SEAforth , modules contain code AND virtual cores… move modules from chip to chip, from application to application, WITHOUT writing drivers and porting hardware
- Eliminates need for floor planning



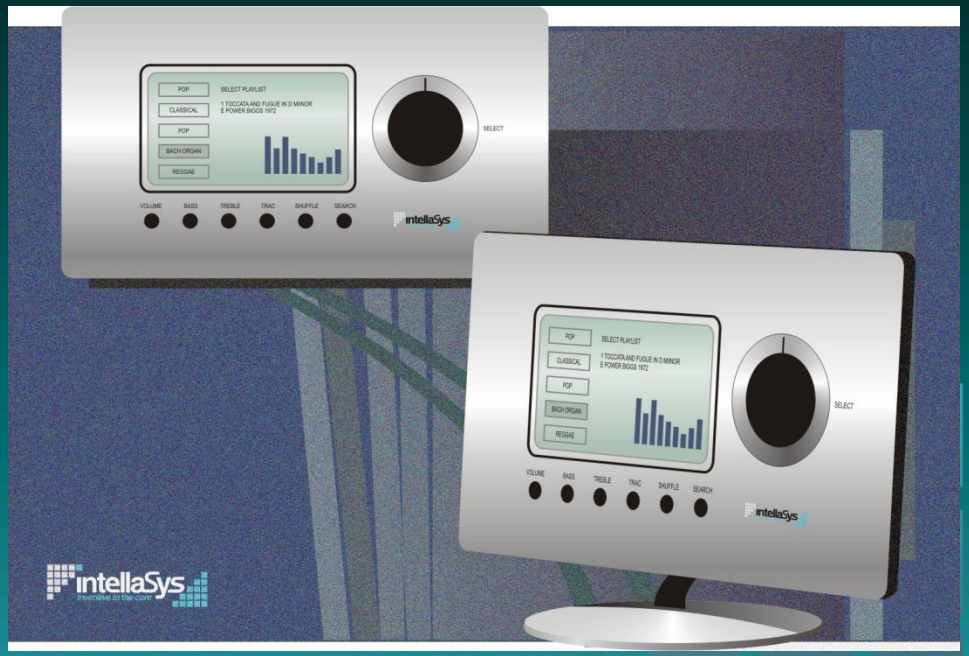
Distributed Digital Media™

- SEAforth chips and code that implement a wirelessly connected consumer environment encompassing home theater and mobile devices
- Low cost, single chip implementations
- Reference designs
  - Complete circuitry and software code for demos
  - Initially provided as VentureForth files ready to download onto SEAforth universal evaluation board
  - May be put into physical prototype later
- Initial List *(but more coming)*
  - Wireless home theater speakers
  - Universal bidirectional remotes
  - Mobile video/audio players

Wireless A/V Receiver

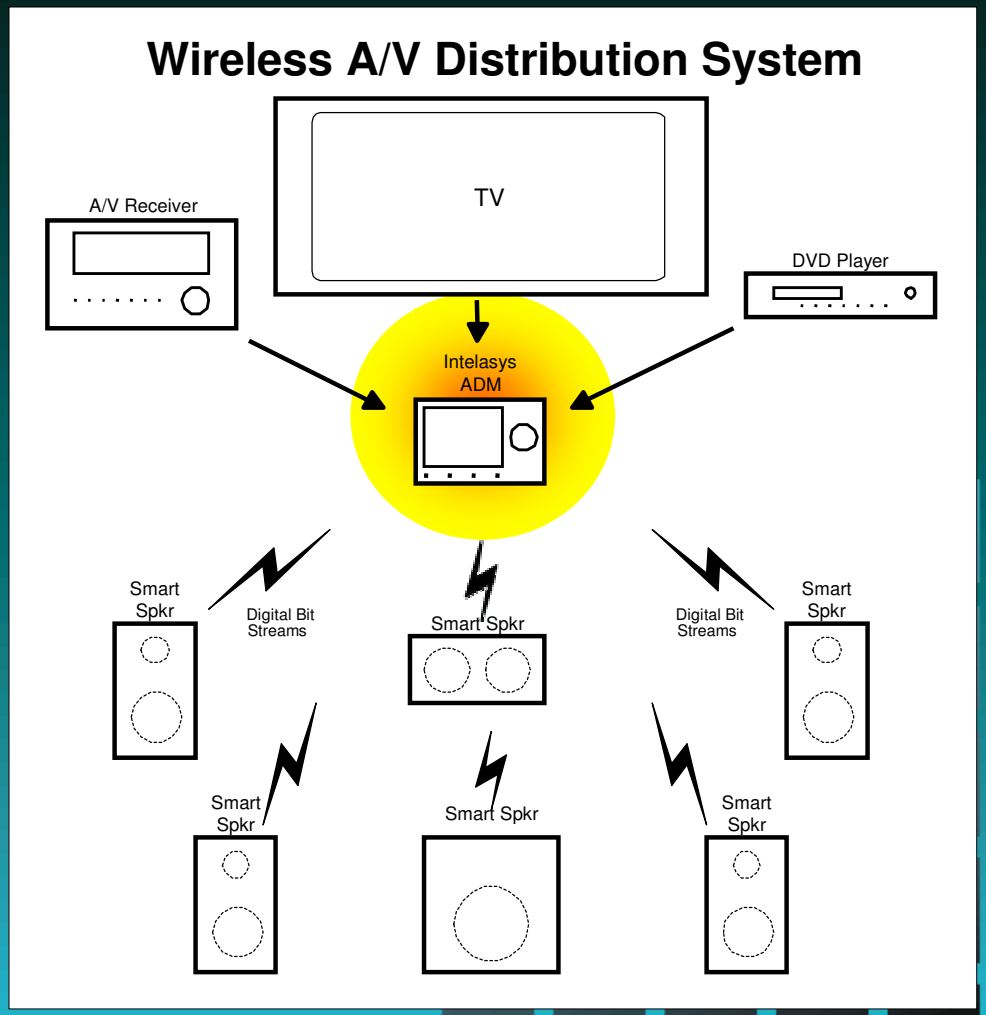
Distributed Digital Media™

- Power amplifiers and large power supply eliminated from A/V receiver
- Provides wireless bidirectional links to six speakers
- Also does MP3 decodes and TCP/IP access to file server



Typical Installation

- 7 SEAforth chips used, one in A/V receiver and one in each speaker
- Speakers extract the appropriate stream
- System can auto calibrate the room and move sweet spot



The SEAforth Advantage

- Low-cost single chip solution to extending wireless capability to speakers… one at A/V receiver and one at each powered speaker
- Eliminates crossover networks at speakers
- Adds MP3 player capability to receiver
- Adds TCP/IP capability to receiver for remote file server access
- Adds bidirectional RF link for SEAforth based remote control

Universal Remote Control

Distributed Digital Media™

- Bidirectional RF link to A/V receiver and home theater components
- Navigate content on RC screen – TV does not have to be ON
- Stereo surround sound headsets driven by RC

Mobile Video Player

Distributed Digital Media™

- H.264 Decoder
- MP3 decoder
- LCD color display
- USB 2.0
- RF link for downloading from file server
- Scriptable GUI

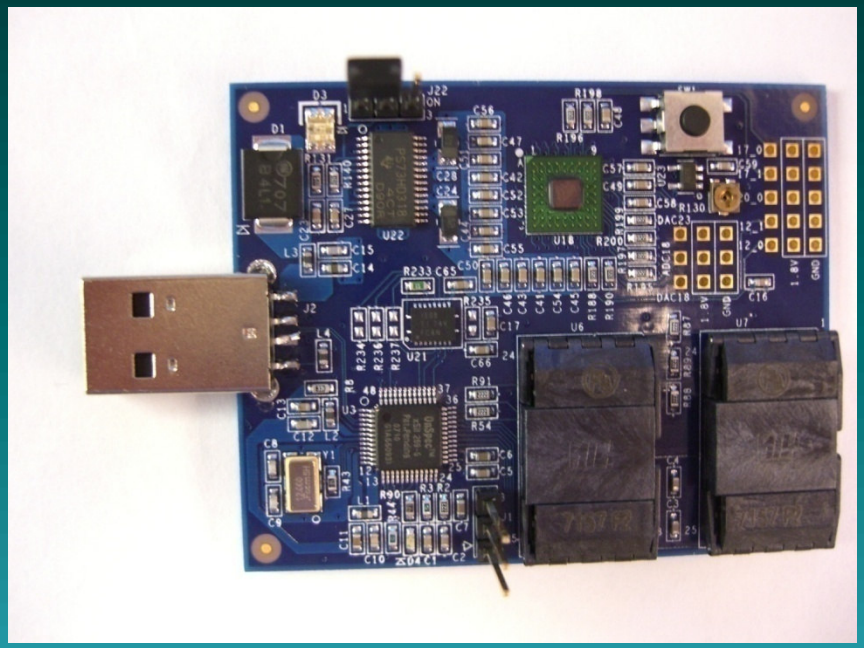
SEAforth Tools
T-18 Compiler / Simulator

- Free download from web right now
- Will be the basis of the SEAforth IDE
  - Write and simulate code on your PC
  - Download to SEAforth hardware platforms like Evaluation thumb drives and evaluation boards
- Develop and debug code today
- Access libraries of VentureForth functions and modules – FIR, DCT, FFT, etc
- Build menus and splash screens
- Windows GUI to be added January 2008
- MATLAB to be added Q1 - 2008

Evaluation Thumb Drive

- SEAforth chip + FLASH + USB Interface
- Plug into laptop and drive with T18
  - Compile code on T18
  - Load code into Thumb FLASH
  - Start SEAforth chip
  - Simple I/O and real time profiling
- Code development platform
  - Every member of your team has a thumb
  - Portable, on-the-go development
  - Adjunct to T18 software simulator
- Available Q3, 2007 (24 core)

Prototyping Boards



- Provide FLASH management plus USB interface
- SOME I/O available
- Low cost
- Customers use for demo purposes
- Derived from prototype of thumb drive

Evaluation Board

- Hardware prototyping tool
- On-board FLASH loaded and controlled from laptop hosting T18 via USB
- Complete platform for a wide range of applications
  - Four SEAforth chips
  - External RAM
  - Extensive analog support
  - Full-color LCD 640x480 VGA color screen
  - LCD touch screen
- Runs demo applications downloaded from web
- Available late Q4 - 2007

SEAforth applications vary widely

- Consumer apps like audio headsets, wireless home theater speakers, portable video players, remote controllers, etc
- Automotive applications like multiple bus interfaces, sensor drivers, dashboard controllers, etc
- Military/Aerospace applications like phased-array radars, satellites, remote sensor reporting
- Medical applications like hearing aids
- RF applications like direct RF conversion in the GigaHertz range

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