

Invitation

to the *Joint Complang/TRACES Workshop on*
Trends in Timing Analysis (TiTAn 2009)
21 April 2009

Library E185.1, Argentinierstr. 8, 4th Floor (Centre)

Workshop Programme

Tuesday, 21 Apr. 2009

10:00 Welcome and Opening

10:15 **A Prospect to the Next Version of TuBound**

Adrian Prantl, Vienna University of Technology, Vienna, Austria.

11:00 **An Introduction to OTAWA**

Clément Ballabriga, TRACES/IRIT, Toulouse, France.

Lunch

14:00 **Loop Analysis with oRange**

Marianne de Michiel and *Armelle Bonenfant*, TRACES/IRIT, Toulouse, France.

15:00 **Timing Anomalies as a Challenge for Precise
Worst-Case Execution Time Analysis**

Raimund Kirner, *Albrecht Kadlec*, and *Peter Puschner*, Vienna University of Technology, Vienna, Austria.

15:45 **Avoiding Timing Anomalies using Prefetch Window Padding**

Albrecht Kadlec, Vienna University of Technology, Vienna, Austria.

16:30 **Timing Predictability and Composability**

Peter Puschner and *Raimund Kirner*, Vienna University of Technology, Vienna, Austria.

17:15 Plenary Session and Farewell

Workshop Dinner

Zu dieser Arbeitstagung lädt der *Arbeitsbereich für Programmiersprachen und Übersetzer* am Institut für Computersprachen herzlich ein.

Abstracts of Presentations

A Prospect to the Next Version of TuBound

Adrian Prantl

Vienna University of Technology
adrian@complang.tuwien.ac.at

The safety of our day-to-day life depends crucially on the correct functioning of embedded software systems which control the functioning of more and more technical devices. Many of these software systems are time-critical. Hence, computations performed need not only to be correct, but must also be issued in a timely fashion. Worst case execution time (WCET) analysis is concerned with computing tight upper bounds for the execution time of a system in order to provide formal guarantees for the proper timing behaviour of a system. State-of-the-art WCET analysis tools rely on supporting analyses and manual annotations to provide them with information on the execution behaviour of the program such as loop bounds or maximum recursion depths. Typically, both steps are performed on the binary code of the program. The manual annotation of a binary program, however, imposes high demands on the programmer [1].

With TuBound, we are providing an improved work-flow by lifting manual annotations and supporting analyses to the source code level of a program. The information computed on this level and annotated in the code is then conjointly transformed throughout the compilation and optimization of the program to the binary code level to make it accessible to the WCET analysis component of our TuBound tool [2].

In this talk, we highlight the latest additions such as the constraint-based loop analysis [3].

References

- [1] Raimund Kirner, Jens Knoop, Adrian Prantl, Markus Schordan, and Ingomar Wenzel. WCET Analysis: The Annotation Language Challenge. In *Proceedings 7th Int. Workshop on Worst-Case Execution Time Analysis (WCET 2007)*, 83 - 99, Pisa, Italy, 2007.
- [2] Adrian Prantl, Markus Schordan, and Jens Knoop. TuBound – A Conceptually New Tool for Worst-Case Execution Time Analysis. In *Proceedings 8th Int. Workshop on Worst-Case Execution Time Analysis (WCET 2008)*, 141-148, Prague, Czech Republic, 2008. ISBN: 978-3-85403-237-3.
- [3] Adrian Prantl, Jens Knoop, Markus Schordan, and Markus Triska. Constraint solving for high-level WCET analysis. In *Proceedings of the 18th Int. Workshop on Logic-based methods in Programming Environments (WLPE 2008)*, 77-89, Udine, Italy, 2008.

An Introduction to OTAWA

Clément Ballabriga

Institut de Recherche en Informatique de Toulouse (IRIT)

Université Paul Sabatier

118 Route de Narbonne

F-31062 Toulouse, France

`ballabri@irit.fr`

OTAWA is a freeware application dedicated to the computation of the WCET of programs. More precisely, OTAWA concerns the numerous WCET approaches based on static analyses of the executable program. Unlike many existing usual tools, the choice has been done to avoid specialisation and to produce, instead, a generic and open framework.

WCET computation has always required to pass flow fact information from the user to the computation analysis even with tools including loop bound analyses. From the start of OTAWA and overmore with the use of the oRange, OTAWA has developed a more and more extensible annotation system based on XML file. In the last project, this annotation system has been largely extended to embed timing information and user domain definitions and to locate accurately information in the program and in the execution time.

Loop Analysis with oRange

Marianne de Michiel and **Armelle Bonenfant**

Institut de Recherche en Informatique de Toulouse (IRIT)

Université Paul Sabatier

118 Route de Narbonne

F-31062 Toulouse, France

`{michiel,bonenfant}@irit.fr`

One of the important steps in processing the worst case execution time (*WCET*) of a program is to determine the loops upper bounds. Such bounds are crucial when verifying real-time systems. We will present oRange, our tool which performs a static loop bound analysis associating flow analysis and abstract interpretation. It considers binary operators (+, -, *, /) for the loop increment, nested loops, non-recursive function calls, simple loop conditions (==, !=, <, ≤, >, ≥, &&) and loop upper bound values (instead of intervals). We will present the different steps of the analysis and some results on the Mälardalen benchmark suite.

Timing Anomalies as a Challenge for Precise Worst-Case Execution Time Analysis*

Raimund Kirner, Albrecht Kadlec and Peter Puschner

Vienna University of Technology

`raimund@vmars.tuwien.ac.at`

Timing anomalies add to the complexity of WCET analysis and make it hard to apply divide-and-conquer strategies to simplify the WCET assessment [2]. So far, timing anomalies have been described as a problem that occurs when the WCET of a control-flow graph is computed from the WCETs of its subgraphs, i.e., from a series decomposition. As one of the research contributions within the project “Compiler-Support for Timing Analysis” (COSTA) we extend the state of the art by (i) showing that timing anomalies can as well occur in a parallel decomposition of the WCET problem, i.e., when complexity is reduced by splitting the hardware state space and performing a separate WCET analysis for hardware components that work in parallel, (ii) proving that the potential occurrence of parallel timing anomalies makes the parallel decomposition technique unsafe (i.e., one cannot guarantee that the calculated WCET bound does not underestimate the WCET), and (iii) identifying special cases of parallel timing anomalies for which the parallel decomposition technique is safe. The latter provides an important hint to hardware designers on their way to constructing predictable hardware components [1].

* The research leading to these results has received funding from the Austrian Science Fund (Fonds zur Förderung der wissenschaftlichen Forschung) within the research project “Sustaining Entire Code-Coverage on Code Optimization” (SECCO) under contract P20944-N13 and by the Austrian Science Fund (Fonds zur Förderung der wissenschaftlichen Forschung) within the research project “Compiler-Support for Timing Analysis” (CoSTA) under contract P18925-N13.

References

- [1] Raimund Kirner, Albrecht Kadlec, and Peter Puschner. Precise worst-case execution time analysis for processors with timing anomalies. In *Proc. 21st Euromicro Conference on Real-Time Systems*, Dublin, Ireland, July 2009. IEEE. To appear.
- [2] Raimund Kirner and Peter Puschner. Obstacles in worst-cases execution time analysis. In *Proc. 11th IEEE International Symposium on Object-oriented Real-time distributed Computing*, pages 333-339, Orlando, Florida, May 2008.

Avoiding Timing Anomalies using Prefetch Window Padding

Albrecht Kadlec

Vienna University of Technology
{albrecht}@vmars.tuwien.ac.at

So called timing anomalies are phenomena in processors where changes of the local worst-case execution time (WCET) do not correspond to changes of the global WCET. Timing anomalies are problematic for timing analysis, since they make it challenging to use abstract hardware models that still lead to safe and tight WCET bounds. In this paper, we refine and categorize the conditions for timing anomalies, distinguishing between triggers and amplifiers, which communicate via processor state only. We use that distinction to present the theoretical approaches for countermeasures against timing anomalies. Then we establish a sufficient condition to avoid timing anomalies from pipeline scheduling decisions. Based on this condition, we modify a standard postpass instruction scheduler to avoid the accumulation of timing effects. This modified scheduler is evaluated for several experimental out-of-order architectures using the Mälardalen WCET benchmark suite. The results are promising.

Towards Timing Predictability and Composability*

Peter Puschner and Raimund Kirner

Vienna University of Technology
{peter,raimund}@vmars.tuwien.ac.at

As real-time software is increasing in size and complexity, the need for advanced modeling and analysis capabilities early in the software development process is getting more and more urgent. One particular concern is the lack of sufficient methods and tools to effectively reason about the timing of software in such a way that software systems can be constructed hierarchically from components while still guaranteeing the timing properties [1]. In this talk, we will discuss deficiencies in current real-time embedded hardware and software structures with respect to achieving our goal of composable and compositional timing behavior. To address these deficiencies, we will then discuss programming methods, code generation techniques, and ideas about hardware and software architectures that should help us in achieving a truly timing-composable and compositional engineering process for real-time software systems.

* Parts of the research leading to these results have received funding from the European Community's Seventh Framework Programme [FP7/2007-2013] under grant agreement no. 214373.

References

- [1] Peter Puschner, Raimund Kirner, and Robert G. Pettit. Towards Composable Timing for Real-Time Software. In *Proc. 1st International Workshop on Software Technologies for Future Dependable Distributed Systems*, pages 1-5. IEEE Computer Society CPS, Mar. 2009.

About the Speakers

- **Ass.-Prof. Dr. Armelle Bonenfant**
Institut de Recherche en Informatique de Toulouse (IRIT),
Université Paul Sabatier,
118 Route de Narbonne, F-31062 Toulouse, France
bonenfant@irit.fr
<http://www.irit.fr/recherches/ARCHI/MARCH/index.php3>
- **Ass.-Prof. Dr. Marianne De Michiel**
Institut de Recherche en Informatique de Toulouse (IRIT),
Université Paul Sabatier,
118 Route de Narbonne, F-31062 Toulouse, France
michiel@irit.fr
<http://www.irit.fr/recherches/ARCHI/MARCH/index.php3>
- **Clément Ballabriga, M.Sc.**
Institut de Recherche en Informatique de Toulouse (IRIT),
Université Paul Sabatier,
118 Route de Narbonne, F-31062 Toulouse, France
ballabri@irit.fr
<http://www.irit.fr/recherches/ARCHI/MARCH/index.php3>

The research interests of the TRACES team include hardware issues of real-time embedded systems. The main goal is to guarantee that the execution time of an application code meets the system deadlines. We focus on characterizing the temporal properties of components off-the-shelves. Our target is to propose ways to use these components such that safe and tight worst-case execution time estimates can be computed. We also study architectural extensions that should improve the time predictability of the components. The estimation of the WCET requires three steps: a static analysis of the code identifies all the possible execution paths; the target hardware is modelled to determine the individual execution times of the basic blocks; then, the results of the previous steps are combined to evaluate an upper bound of the global execution time. Part of our work concerns the first and second steps.

Marianne de Michiel is an assistant professor; she works especially on loop bounds. Clément Ballabriga is a PhD student supervised by Hugues Cassé since 2006 and works on cache behavior, partial analysis and abstract interpretation. Armelle Bonenfant joined the team in 2007 and collaborates with Marianne de Michiel.

- **Dipl.-Ing. Albrecht Kadlec**
Institute of Computer Engineering
Vienna University of Technology
A-1040 Vienna, Austria
albrecht@vmars.tuwien.ac.at
<https://ti.tuwien.ac.at/rts>

Albrecht Kadlec holds a MSc Degree in automation and compilers from TU Vienna. He has been working for seven years in the embedded compiler industry. In 2007 he left Mentor Graphics to join the CoSTA (Compiler Support for Timing Analysis) team as a PhD research assistant.

- **Dr. Raimund Kirner**
Institute of Computer Engineering
Vienna University of Technology
A-1040 Vienna, Austria
raimund@vmars.tuwien.ac.at
<https://ti.tuwien.ac.at/rts>

Univ. Assistent Dr. Raimund Kirner received his Master's degree and his PhD degree at the Vienna University of Technology (TU Vienna) in 2000 respectively 2003. During this time he has been working as a research and teaching assistant at the Institut für Technische Informatik at TU Vienna. The main focus of Kirner's research is worst-case execution time analysis of real-time programs, including compiler support and design methodologies to make systems predictable. He has published several papers on WCET analysis and was involved in two projects funded by the European Commission (SETTA, NEXT TTA). From 2003-2005 Raimund Kirner has worked on the FIT-IT project MoDECS, and from 2005-2007 he worked on the FIT-IT project TeDES, both funded by the Federal Ministry of Transport, Innovation, and Technology (BMVIT). Currently, Raimund Kirner is principal investigator of the following projects: "Compiler-Support for Timing Analysis" (COSTA), "Formal Timing Analysis Suite" (FORTAS), and "Sustaining Entire Code-Coverage on Code Optimization" (SECCO). He is a member of the IEEE Computer Society, the ACM, and the Austrian Computer Society (OCG).

- **Dipl.-Ing. Adrian Prantl**

Institute of Computer Languages
Vienna University of Technology
A-1040 Vienna, Austria
adrian@complang.tuwien.ac.at
<http://www.complang.tuwien.ac.at/adrian>

Adrian Prantl studied computer science at the Vienna University of Technology. During the final year he worked with OnDemand Microelectronics designing and implementing the compiler tool chain for the Chili family of VLIW processors. He is currently working towards a PhD and engaged in the FWF-funded project “Compiler Support for Timing Analysis” (CoSTA) aiming at bringing the power of source code transformations to the field of worst-case execution time analysis.

- **Prof. Dr. Peter Puschner**

Institute of Computer Engineering
Vienna University of Technology
A-1040 Vienna, Austria
peter@vmars.tuwien.ac.at
<https://ti.tuwien.ac.at/rts>

Peter Puschner is a professor in computer science at Vienna University of Technology. His main research interest is on hard real-time systems for safety-critical applications, with a focus on the worst-case execution time (WCET) analysis of real-time programs and software/hardware architectures for time-predictable computing. He has published more than 80 refereed conference and journal papers and was a guest editor for the special issue on WCET analysis of the Kluwer (now Springer) International Journal on Real-Time Systems in 2000. P. Puschner chaired the PC of ISORC 2003 and ECRST 2004 and was the general chair of the Euromicro Conference on Real-Time Systems 2002 and ISORC 2004. He is in charge of the steering committees of the workshop series on worst-case execution-time analysis (WCET) and the International Workshop on Software Technologies for Future Embedded and Ubiquitous Computing Systems (SEUS). P. Puschner is a member of the IEEE Computer Society, IFIP working group 10.2 on Embedded Systems, Euromicro, the OCG (Austrian Computer Society), and the Marie-Curie Fellowship Association.