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Limited Address Range Architecture for Reducing Code Size in Embedded Processors

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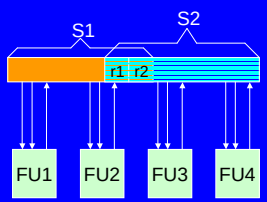
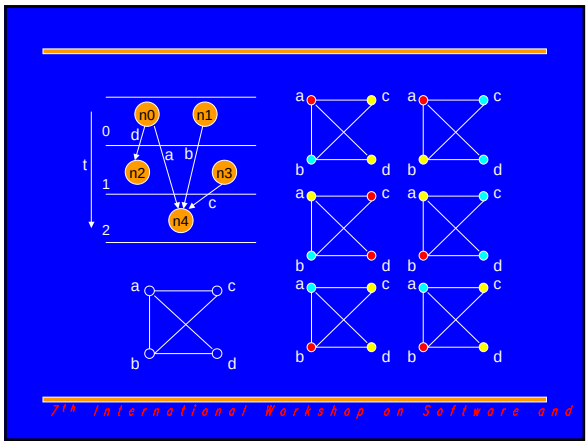
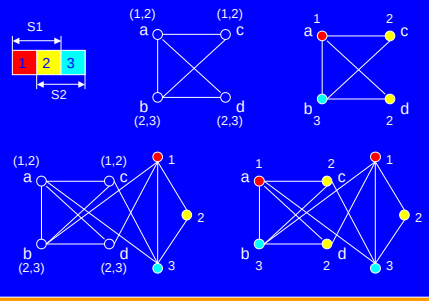
- Introduction
  - Code size, power consumption of embedded cores must be small since they are on chip
  - Irregularities in architectures
    - Difficult for efficient code generation
  - Clustered register file vs. central register file
    - Advantage: small code size, power consumption
    - Disadvantage: extra hardware, copy operations
  - Phase coupling in code generation
    - Sequential phases may generate inefficient code
    - Integrated approach potentially offers better solutions





– Annotated Conflict Graph(ACG)



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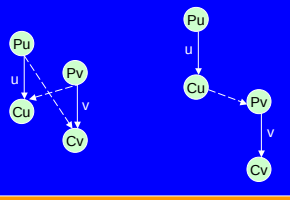
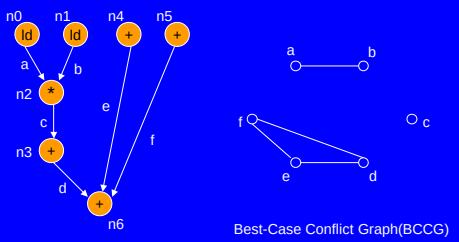
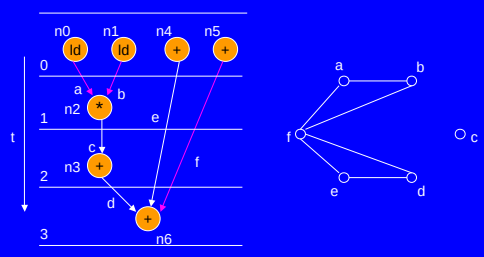
- The proposed architecture: LAR
- Sequential code generation for LAR
  - Annotated Conflict Graph(ACG)
- The integrated approach
  - Annotated Worst-Case Conflict Graph(AWCCG)
- Experimental results
- Conclusions and future work

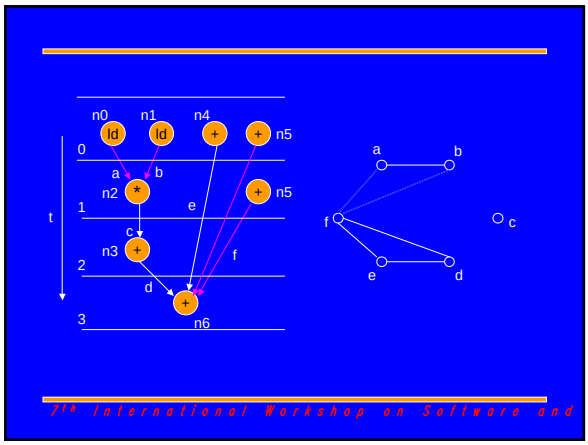
- Lifetime conflict:
  - Strong conflict: *u* and *v* overlap for sure
  - No conflict: *u* and *v* can never overlap
  - Weak conflict: neither of the above holds

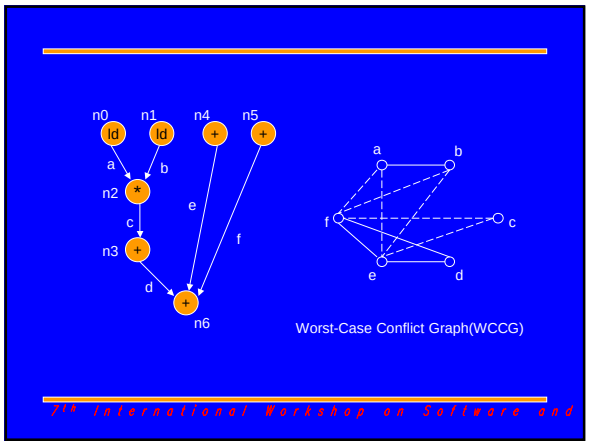




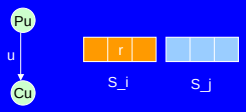
Best-Case Conflict Graph(BCCG)

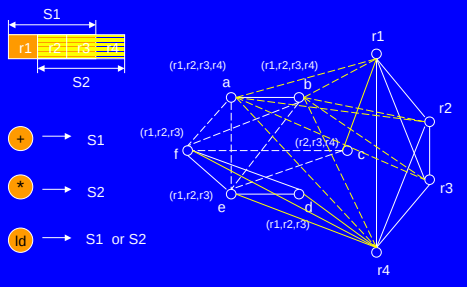




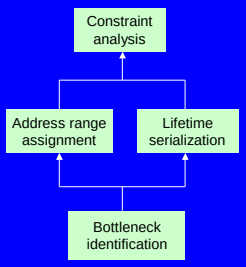


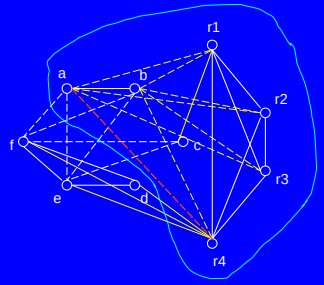
- Range assignment conflict:
  - Strong conflict: *u* and *r* have strong conflict if *u* can never reside in *S_i*, where *r* in *S_i*
  - No conflict: *u* and *r* have no conflict if *u* can always reside in *S_i*, where *r* in *S_i*
  - Weak conflict: *u* and *r* have weak conflict if *u* can reside in *S_j*, where *r* notin *S_i*

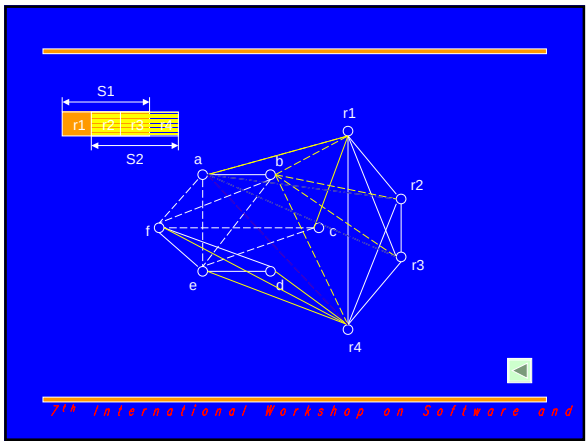


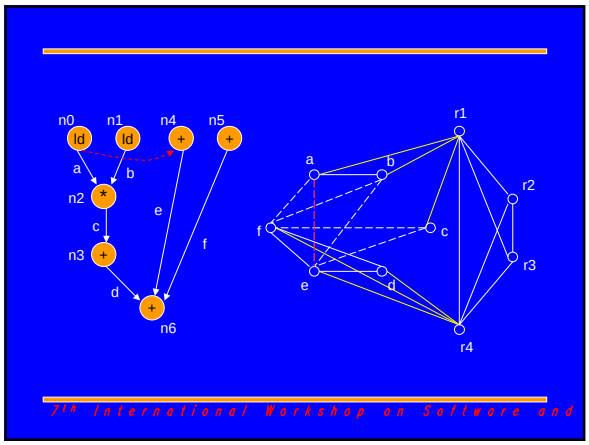


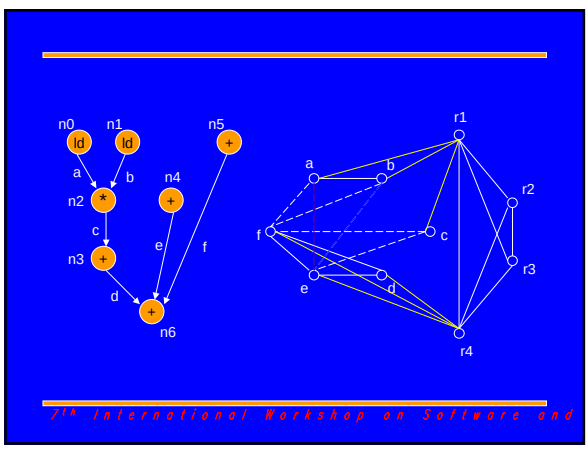
– Overview of the integrated approach











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DFG_fu,l	encoding			sequential			integrated		
	central	LAR	%	|S|	|S_o|	T(s)	|S|	|S_o|	T(s)
ar_filter_1,18	392	308	78.57	5	2	0.07	5	2	0.09
wdelf_1,27	476	388	83.61	6	2	0.07	6	2	0.12
fdct_2,20	714	588	82.35	9	5	inf	9	5	4.95
fdct_4,11	714	588	82.35	9	6	inf	9	6	0.35
				9	7	0.26	9	7	0.37
loef_2,15	952	952	100	12	7	0.95	12	7	no
				12	8	inf	12	8	1.43
				12	9	0.2	12	9	no
loef_4,11	952	952	100	12	9	inf	12	9	0.89
chen_2,15	680	560	82.35	8	4	inf	8	4	1.28
				8	5	0.24	8	5	4.28
				9	3	0.22	9	3	no
chen_4,8	680	560	82.35	9	4	0.19	9	4	0.24
				9	5	0.18	9	5	0.24

- Conclusions and future work
  - Conclusions
    - New encoding style for reducing code size
    - No extra hardware, no extra move operations
    - Corresponding code generation techniques
    - ACG for range constraints
    - AWCCG solves phase coupling problem
  - Future work
    - More versatile architectures
    - Combine with the operation assignment phase