

Time-predictable Computer Architecture to Simplify Worst-Case Execution Time Analysis

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Abstract. Standard processors are optimized for performing best in the average case. Out-of-order pipelines, speculation, and several levels of caches are example features that improve average case execution time. However, for real-time systems we are interested in the worst-case execution time (WCET). And exactly those features that improve average case performance are problematic for the WCET. They may increase the WCET and they may be hard, or even impossible, to model for WCET analysis. In this paper we present a new line of computer architecture research where the main optimization point is for the WCET and especially to simplify WCET analysis.