

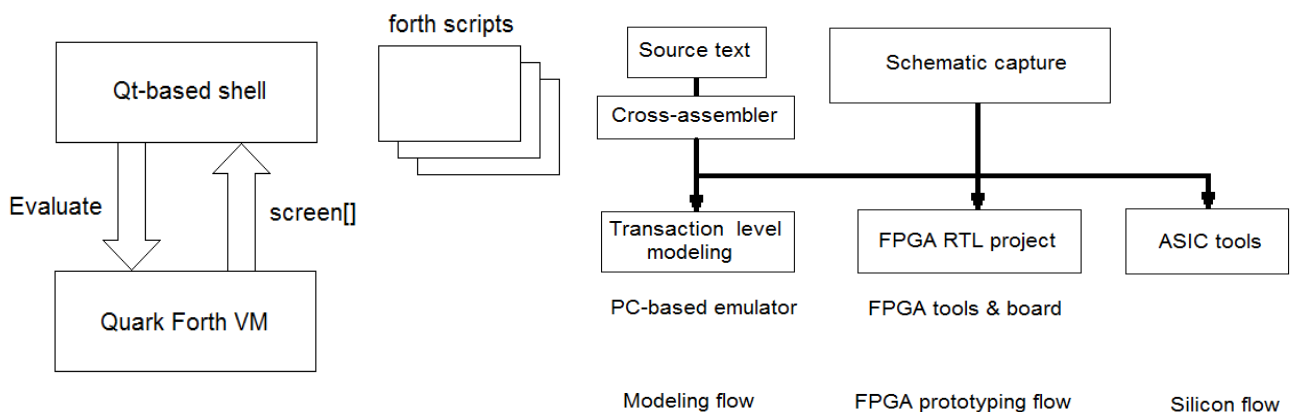
A Forth-Based CAD for System-Level Microelectronic Design

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This article describes features of use of the Forth-based engine for the decision of a problem of creation microelectronic CAD. This project is carried out under a state contract, supported by the Ministry of Science and Education of the Russian Federation.

- Early integration of embedded software, that enables complex hardware and software cosimulation.
- Modeling at the transaction level (TLM, Transaction Level Modeling).
- Integration with industry standard software tools, such as topology-level CAD software, and, from the other side, mathematical and DSP software tools and high-level languages.
- Using script languages for automated creation of a project and running the design flow in a batch mode.

Quark-Forth, a C++ based Forth engine, interacts with Qt shell and providing a design flow



Quark CAD stack processor cores (included in a component library)

The RISC-processor, named QuarkR, is a 32-bit general-purpose processor.

- Harvard architecture with a 3-stage pipeline
- 32 general-purpose registers
- 3-address and stack-based register file access, when the top of data stack is initially located in R31
- Independent return stack (32 cells deep), switchable to a stack in the external data memory
- 32-bit wide command
- Base Forth commands implemented in hardware as a command set extension (no mode switching is required)

DSP:

- Independently running MAC engines, 1 or 2 blocks in each DSP core.
- Control processor unit, 32-bit stack core with 8-bit wide commands; command set is similar to that of QuarkR

Matrix processor

- 4 cells deep data stack, 4 cells deep return stack
- Harvard architecture with separate code and data memories for each core
- Up to 32x32 processor unit grid
- Local links, global column buses and system bus interface

