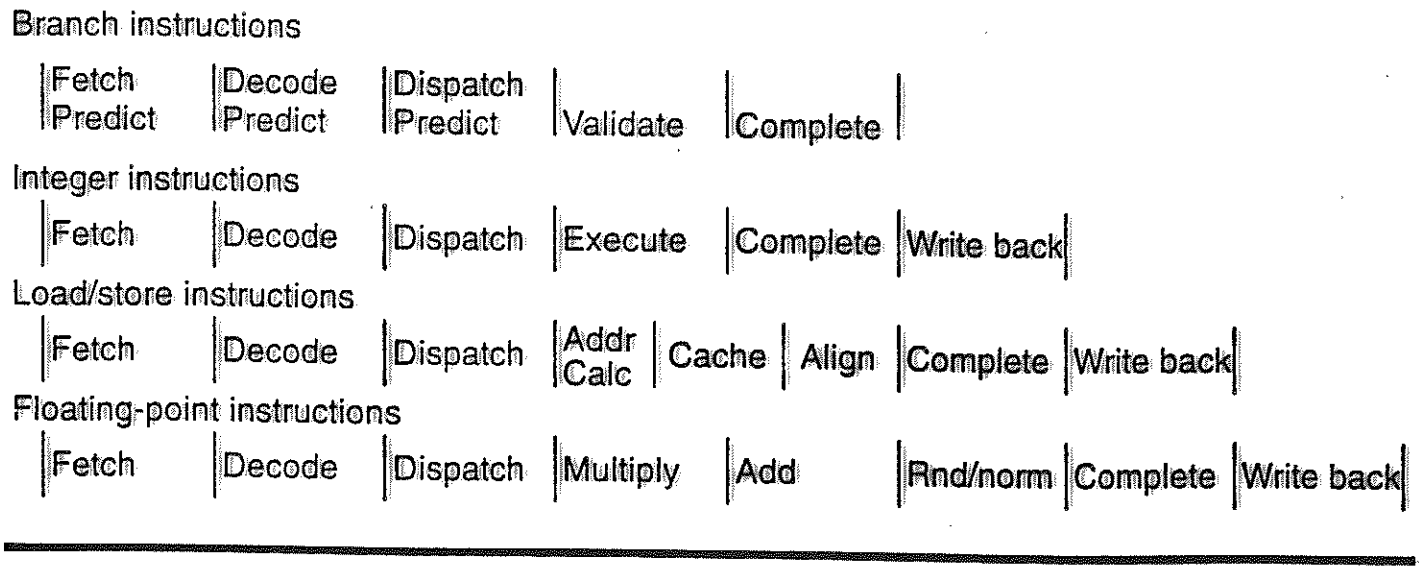


Figure 1. Pipeline description.

Table 1. 604 execution timings.

Instruction	Latency	Throughput
Most integer	1	1
Integer multiply (32×32)	4	2
Integer multiply (others)	3	1
Integer divide	20	19
Integer load	2	1
Floating-point load	3	1
Store	3	1
Floating-point multiply-add	3	1
Single-precision floating-point divide	18	18
Double-precision floating-point divide	31	31

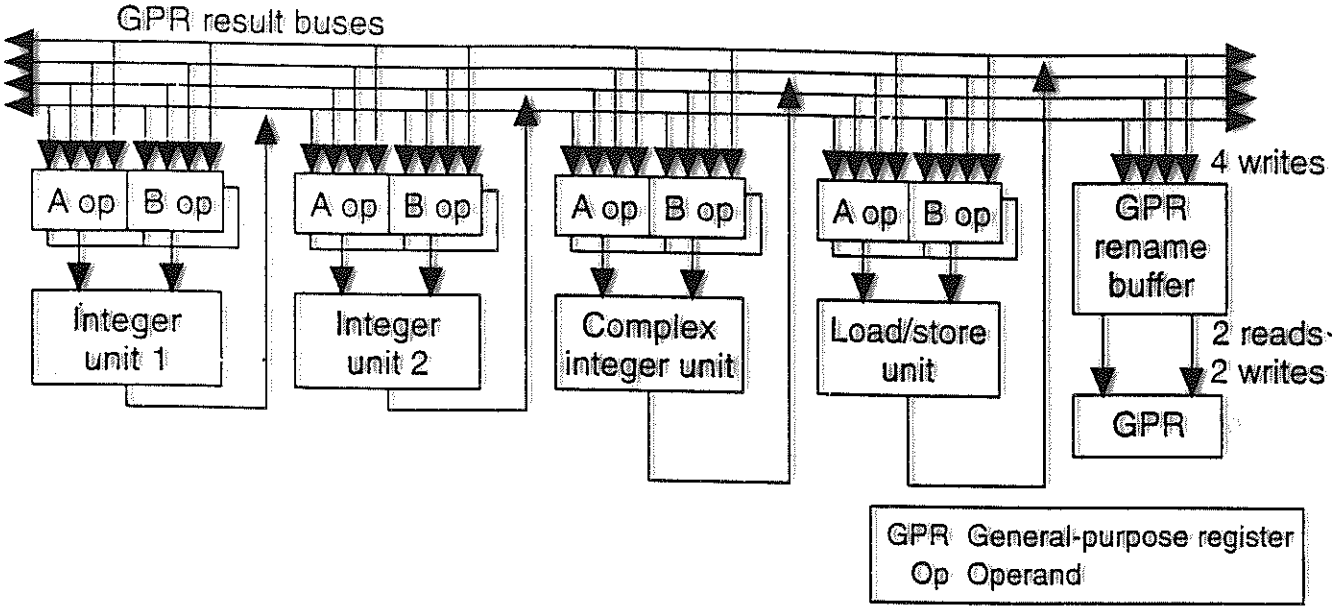


Figure 4. GPR result buses, reservation stations, and rename buffer.

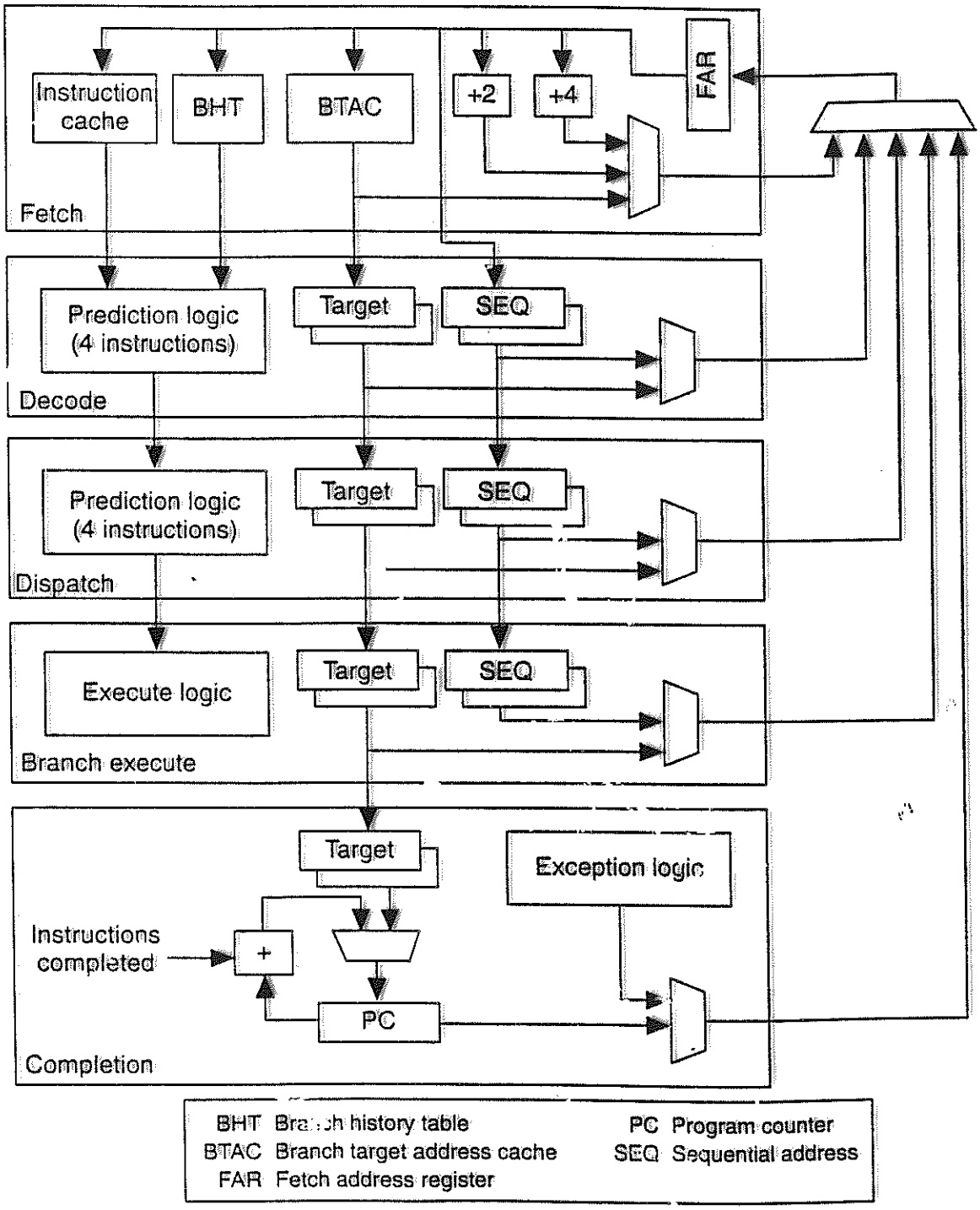
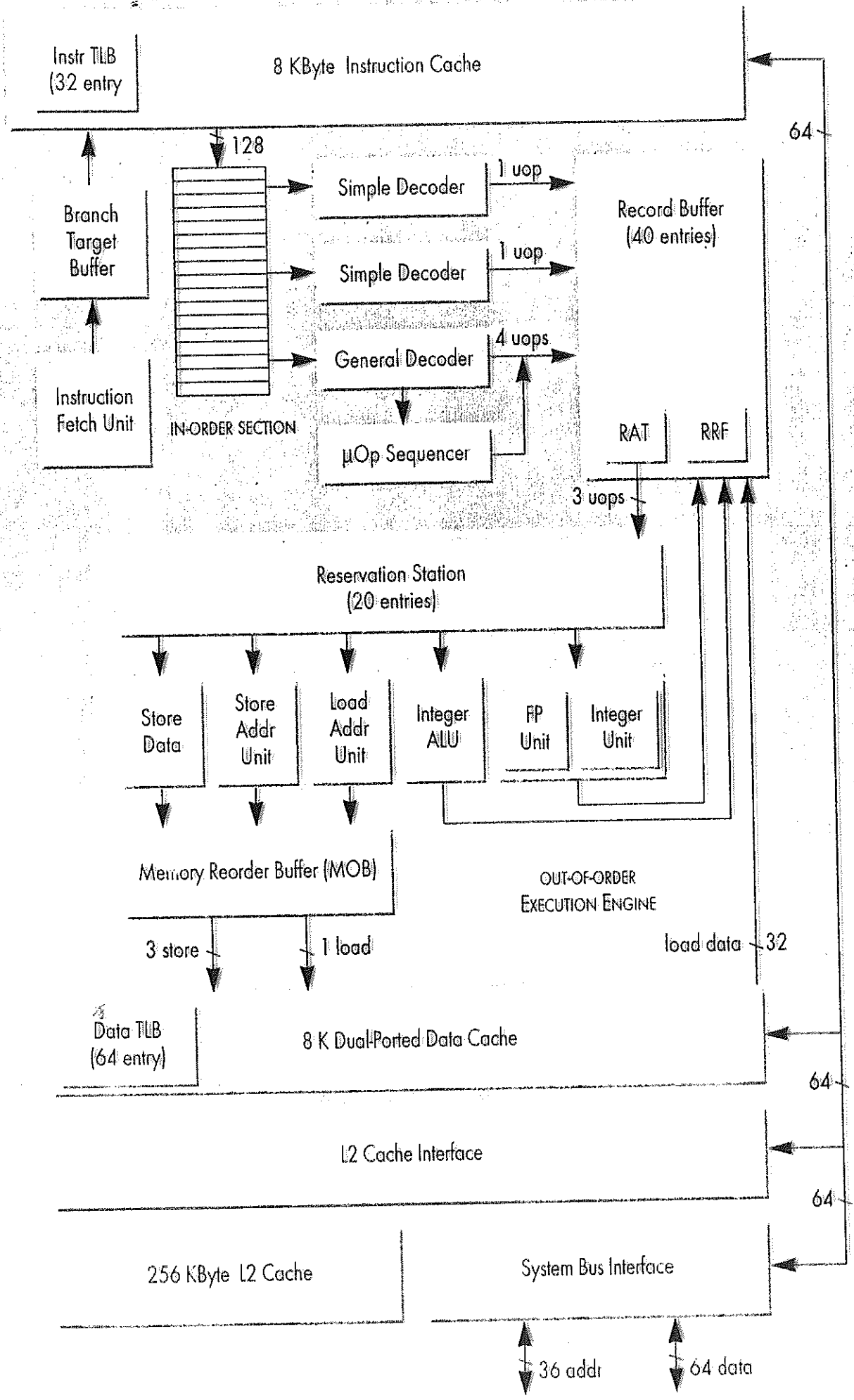


Figure 3. Instruction fetch address generation logic.



Das Blockschaltbild zeigt den Aufbau des P6. Der innere, dunkel unterlegte Prozessorteil verarbeitet die Befehle 'out of order', im äußeren Bereich werden