CGO-5 - CALL FOR PARTICIPATION

Preliminary Program

Online Registration is open: `http://www.cgo.org`

Fifth Annual IEEE/ACM International Symposium on CODE GENERATION and OPTIMIZATION (CGO-5)

11-14 March 2007 - San Jose, California
`http://www.cgo.org`

Important Dates:

- Advance registration deadline: **26 February 2007, 5:00 pm EST**.
  After this date, onsite registration only – Late fees apply.
- Conference cancellation deadline: **26 February 2007**.
- Hotel reservation deadline: **19 February 2007**.
- Visa information: Please note the information for foreign registrants of CGO-5 at `http://www.cgo.org`.

CGO-5 Preliminary Program

(Please note that this preliminary schedule might be subject to change. Please stay tuned and make sure that you come back to `http://www.cgo.org` for last minute updates).

CGO-5 Invited Keynote Talks

- **Ian Buck**, NVIDIA, GPU-Compute Software Manager, on
  "GPU Computing: Programming a Massively Parallel Processor"
  Time: Tuesday morning.
- **Jesse Fang**, Intel, Director of Programming Systems Lab, on
  "Parallel Programming Environment: A Key to Translating Tera-Scale Platforms into a Big Success"
  Time: Wednesday after joint CGO/PPoPP lunch.

Sunday, 11 March 2007

Workshops

- **ODES**: 5th Workshop on Optimizations for DSP and Embedded Systems
- **STMCS**: Second Workshop on Software Tools for Multi-Core Systems
- **EPIC-6**: Workshop on EPIC Architectures and Compiler Technology
- **Workshop** on Data-Parallel Programming Models for Many-Core Architectures

Tutorials

- *Practical Phoenix: A Hands-On Tutorial*
  Andy Ayers (Microsoft Phoenix), **Yan Xu** (Microsoft Research)
- *GCC Internals*
  Diego Novillo (Red Hat Canada)
- *Open64: the Open-Source High-Performance Compiler for Servers, Embedded Systems and Compiler/Architecture Research*
  Shin-Ming Liu (HP), **Pen-Chung Yew** (University of Minnesota), **Sun Chan** (Simplight Nanoelectronics), **Shengyuan Wang** (Tsinghua University), **Yuan Dong** (Tsinghua University)

Monday, 12 March 2007

08:00-08:15 Welcome

08:15-09:15 Session 1: Transactions
Chair: Christos Kozyrakis, Stanford University

Understanding Tradeoffs in Software Transactional Memory.
Dave Dice (Sun Microsystems) and Nir Shavit (Sun Microsystems and Tel-Aviv University)

Code Generation and Optimization for Transactional Memory Constructs in an Unmanaged Language.
Cheng Wang (Intel Corporation), Wei-Yu Chen (University of California, Berkeley), Youfeng Wu, Bratin Saha, and Ali-Reza Adl-Tabatabai (Intel Corporation)

09:45-11:15 Session 2: Run-Time Optimization and JIT
Chair: Cliff Click, Azul Systems

Run-Time Support for Optimizations Based on Escape Analysis.
Thomas Kotzmann and Hanspeter Mössenböck (Johannes Kepler University Linz)

Evaluating Indirect Branch Handling Mechanisms in Software Dynamic Translation Systems.
Jason D. Hiser, Daniel Williams, Wei Hu, Jack W. Davidson (University of Virginia), Jason Mars, and Bruce R. Childers (University of Pittsburgh)

Persistent Code Caching: Exploiting Code Reuse across Executions and Applications.
Vijay Janapa Redd (Harvard University), Dan Connors (University of Colorado at Boulder), Robert Cohn (Intel), and Michael D. Smith (Harvard University)

11:45-12:45 Lunch

13:15-14:45 Session 3: Optimization I
Chair: Teresa Johnson, Hewlett Packard

Virtual Cluster Scheduling through the Scheduling Graph.
Josep M. Codina (UPC and Intel Barcelona Research Center), Jesús Sánchez (Intel Barcelona Research Center, UPC), and Antonio González (UPC and Intel Barcelona Research Center)

On the Complexity of Register Coalescing.
Florent Bouchez, Alain Darte, and Fabrice Rastello (LIP UMR CNRS-ENS Lyon-UCB Lyon-Inria)

A Dimension Abstraction Approach to Vectorization in Matlab.
Neil Birkbeck, Jonathan Lévesque, and José Nelson Amaral (University of Alberta)

15:15-17:15 Session 4: Guiding Optimizations
Chair: Andy Ayers, Microsoft

Microarchitecture Sensitive Empirical Models for Compiler Optimizations.
Kapil Vaswani, Matthew J. Thazhuthaveetil, Y. N. Srikant (Indian Institute of Science, Bangalore), and P. J. Joseph (Freescale, India)

Iterative Optimization in the Polyhedral Model: Part I, One-Dimensional Time.
Louis-Noel Pouchet, Cédric Bastoul, Albert Cohen, and Nicolas Vasilach (INRIA FUTURS and Paris-Sud University)

Evaluating Heuristic Optimization Phase Order Search Algorithms.
Prasad A. Kulkarni, David B. Whalley, Gary S. Tyson (Florida State University), and Jack W. Davidson (University of Virginia)

Loop Optimization Using Hierarchical Compilation and Kernel Decomposition.
Barthou Denis (Université de Versailles Saint-Quentin), Sebastien Donadio (Université de Versailles Saint-Quentin and BULL SA), Patrick Carribault (BULL SA, LRC ITACA, CEA/DAM, Université de Versailles Saint-Quentin), Alexandre Duchateau (LRC ITACA, CEA/DAM, Université de Versailles Saint-Quentin), and William Jalby (Université de Versailles and LRC ITACA, CEA/DAM)

17:30-18:00 Reception

18:00-19:00 Panel Discussion:
Chairs: Michael Paleczny, Sun and Carol Eidt, Microsoft

"Are new languages necessary for multicore?"

19:00-21:00 Dinner on your own

21:00 Business Meeting

Tuesday, 13 March 2007

08:30-09:30 Keynote Address
Chair: Christos Kozyrakis, Stanford University

Ian Buck, NVIDIA, GPU-Compute Software Manager, on
"GPU Computing: Programming a Massively Parallel Processor"

10:00-11:30 Session 5: Profiling and Instrumentation
Chair: Michael Paleczny, Sun

Rapidly Selecting Good Compiler Optimizations Using Performance Counters.
John Cavazos (University of Edinburgh), Grigori Fursin (INRIA Futurs and Paris-Sud University), Felix Agakov, Edwin Bonilla, Michael F. P. O'Boyle (University of Edinburgh), and Olivier Temam (INRIA Futurs and Paris-Sud University)

Shadow Profiling: Hiding Instrumentation Costs with Parallelism.
Tipp Moseley, Alex Shye, Vijay Janapa Reddi, Dirk Grunwald (University of Colorado at Boulder), and Ramesh Peri (Intel Corporation)

SuperPin: Parallelizing Dynamic Instrumentation for Real-Time Performance.
Steven Wallace (Intel Corporation) and Kim Hazelwood (University of Virginia)

11:30-13:30 Lunch on your own

13:30-15:00 Session 6: Special Issues
Chair: Jens Knoop, TU Vienna, Austria

Compilation Techniques for Real-Time Java Programs.
Mike Fulton and Mark Stoodley (IBM Canada)

Compiler-Directed Variable Latency Aware SPM Management to Cope with Timing Problems.
O. Ozturk, G. Chen, M. Kandemir (Pennsylvania State University), and M. Karakoy (Imperial College)

Compiler-Managed Software-Based Redundant Multi-threading for Transient Fault Detection.
Cheng Wang, Ho-seop Kim, Youfeng Wu, and Victor Ying (Intel Corporation)

15:30-17:00 Session 7: Optimization II
Chair: Nacho Navarro, UPC, Spain

Graph-Based Procedural Abstraction.
A. Dreweke, M. Wörlein (University of Erlangen-Nuremberg), I. Fischer (University of Konstanz), D. Schell (University of Erlangen-Nuremberg), T. Meinl (University of Konstanz), and M. Philippsen (University of Erlangen-Nuremberg)

Structure Layout Optimization for Multithreaded Programs.
Easwaran Raman (Princeton University), Robert Hundt, and Sandya S. Mannarswamy (Hewlett-Packard)

Code Compaction of an Operating System Kernel.
Haifeng He, John Trimble, Somu Perianayagam, Saumya Debray, and Gregory Andrews (University of Arizona)

17:30-21:00 Evening at Google

Wednesday, 14 March 2007

08:00-09:30 Session 8: Memory Optimizations
Chair: Olof Lindholm, BEA

Ubiquitous Memory Introspection.
Qin Zhao (Singapore-MIT Alliance and National University of Singapore), Rodric Rabbah (IBM T.J. Watson Research Center), Saman Amarasinghe, Larry Rudolph (Singapore-MIT Alliance, Massachusetts Institute of Technology), and Weng-Fai Wong (Singapore-MIT Alliance and National University of Singapore)

Pipelined Execution of Critical Sections Using Software-Controlled Caching in Network Processors.
Jinquan Dai, Long Li, and Bo Huang (Intel China Software Center)

Isla Vista Heap Sizing: Using Feedback to Avoid Paging.
Chris Grzegorczyk, Sunil Soman, Chandra Krintz, and Rich Wolski (University of California at Santa Barbara)

10:00-11:30 Session 9: Novel Architectures
Chair: Carol Eidt, Microsoft

Exploiting Narrow Accelerators with Data-Centric Subgraph Mapping.
Amir Hormati, Nathan Clark, and Scott Mahlke (University of Michigan-Ann Arbor)

Heterogeneous Clustered VLIW Microarchitectures.
Àlex Aletà (UPC), Josep M. Codina, Antonio González (UPC and Intel Barcelona Research Center), and David Kaeli (Northeastern University)

Profile-Assisted Compiler Support for Dynamic Predication in Diverge-Merge Processors.
Hyesoon Kim, José A. Joao (University of Texas at Austin), Onur Mutlu (Microsoft Research), and Yale N. Patt (University of Texas at Austin)

11:30-12:00 CGO Closing

12:30-13:00 CGO/PPoPP Joint Lunch

13:00-14:00 Keynote Address
Chair: Ali-Reza Adl-Tabatabai, Intel

Jesse Fang, Intel, Director of Programming Systems Lab, on
"Parallel Programming Environment: A Key to Translating Tera-Scale Platforms into a Big Success"

`+++ Afterwards: Start of PPoPP 2007: http://www.ppopp.org/ +++`

CGO-5 Homepage: `http://www.cgo.org/`